CLAIMS:

1. An integrated circuit (14) with an application circuit (1) to be tested and a self-testing circuit (5-13), which is provided for testing the application circuit (1) and generates pseudorandom test patterns, which can be transformed, by means of first logic gates (6, 7, 8) and signals externally fed to said gates, into deterministic test vectors, which are fed to the application circuit (1) for testing purposes, wherein the output signals occurring through the application circuit (1) as a function of the test patterns are evaluated by means of a signature register (13), wherein, by means of second logic gates (10, 11, 12) and signals externally fed to said gates, those bits of the output signals of the application circuit (1) which, due to the circuit structure of the application circuit (1), have undefined states, are blocked during testing.

2. An integrated circuit as claimed in claim 1, characterized in that, within the self-testing circuit (5-13), a linear, feedback shift register (5) is provided, which generates pseudorandom test patterns, which are transformed into predeterminable deterministic test patterns, by means of the first logic gates (6, 7, 8).

3. An integrated circuit as claimed in claim 1, characterized in that the second logic gates (10, 11, 12) block those bits of the output signals of the application circuit (1) that are influenced by those circuit elements of the application circuit (1) which have an analog behavior and/or a storage behavior.

4. An integrated circuit as claimed in claim 1, characterized in that the signals externally fed to the first (6, 7, 8) and second (10, 11, 12) logic gates originate from a test arrangement (15) provided outside the integrated circuit.